22nd IEEE European Test Symposium (ETS) 2017
22-26 May 2017, Limassol, Cyprus

"The IEEE European Test Symposium (ETS) is Europe's premier forum dedicated to presenting and discussing scientific results, emerging ideas, applications, hot topics, and new trends in the area of electronic-based circuits and system testing and reliability." This year, ETS took "place at Amathus Beach Hotel, Limassol, Cyprus, organized by the University of Cyprus, which co-sponsored the event jointly with the IEEE Council on Electronic Design Automation (CEDA)."

"ETS traditionally enjoys a strong balance among academic and industrial participants. In addition to regular Scientific Papers, Special Sessions, Panels, and Embedded Tutorials, ETS features Vendor Sessions and Table-Top Demos, a special track on Emerging Test Strategies (ETS2) where new issues are presented by the industry and are discussed in an informal atmosphere, as well as the new initiative of Industry Wish List where industry presents elevator talks on open issues that demand urgent solutions. ETS is the major event of the European Test Week that includes TSS (Test Spring School) and fringe workshops."

In the main Symposium event, on 23rd of May 2017, I presented the poster for our accepted paper, titled "**Automated Area and Coverage Optimization of Minimal Latency Checkers**" (going to be indexed on IEEE Xplore). In this work, we have addressed the problem of obtaining and optimized set of checkers (fault monitors) in terms of fault coverage and area based on an initial set of checkers. Two different heuristics are used to minimize the checkers, one always providing an exact solution, but not being scalable, while the other is scalable, and still provides an acceptable solution. As an example, the proposed automated framework, which is applied to the control part of an open-source Network-on-Chip router. As opposed to duplication/triplication based approaches, concurrent online checkers provide fault localization information.

In addition, on 26th of May 2017, during one of the workshops as part of the symposium, named RESCUE Workshop, I presented the poster for another accepted paper, titled "**On Fault Detection Efficiency of Reliability Checkers Obtained by Verification Assertion Qualificatio**n". In this work, "correlation between verification assertion qualification results and gate-level fault detection capabilities of concurrent error checkers synthesized from these assertions" is assessed. An industry tool, named Certitude is utilized in order to quality verification assertions. Afterwards, a minimization greedy algorithm is used to generate low-area high quality checkers. "Finally, the fault detection capabilities of the obtained checkers are evaluated using the framework developed by the authors of the paper. This is the first work to consider correlation of assertion quality versus fault detection

capabilities of the synthesized checkers. It is also the first time when qualified assertions are minimized with considerations of the checker coverage and overhead area."

In overall, the main conference and also the workshop was a great opportunity to be updated about state of the art in the field of testing and research related to reliability and fault tolerance and dependability aspects of digital circuits which would also have overlap with our current research direction. I also had the opportunity to talk to different professors and staff from industry in this field, while also being able to discuss overlapped topics of research with other PhD students who attended this event. I would also like express my gratitude to Tallinn University of Technology and IT Academy programme (sponsored by Skype) for sponsoring me and making it possible to attend the event, which could also have positive effects on my future research and possible career path.

May 28th 2017
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