This report presents a scientific overview of the two conferences I attended between 7th and 15th of June 2017. The first conference is *European Association for Education in Electrical and Information Engineering* while the second is Mediterranean Conference on Embedded Computing.

The **EAEEIE (*European Association for Education in Electrical and Information Engineering*)** is a European non-profit organization, with members from nearly seventy European Universities, most of them teaching in the area of *Electrical and Information Engineering* (EIE).

The conference brought together lecturers, researchers and professionals in the field of EIE all over Europe with the aim to exchange ideas and information and contribute to the development of EIE education. The 27th edition of the conference took place in Grenoble, France and was organized by Univ. Grenoble Alpes and Grenoble-INP and took place between 7th and 9th of June 2017. http://eaeeie2017-iut1.univ-grenoble-alpes.fr/

At EAEEIE conference, I presented my paper titled Teaching Digital System Test, co-authored by Raimund Ubar and Margus Kruus. In the paper, we proposed a novel concept of teaching how to test complex digital systems. A set of methods and tools were presented to support laboratory scenarios for test generation and test quality evaluation for microprocessor systems. The paper contributes to providing new tools and materials for computer engineering education with the goal to solve innovative system design and test tasks as part of learning and education.

The second conference is the 6th ***Mediterranean Conference on Embedded Computing (MECO 2017)*** which is an International Scientific Forum aimed to present and discuss the leading achievements in the modeling, analysis, design, validation and application of embedded computing systems. Meco 2017 took place in Bar, Montenegro between 11th and 15th of June 2017. http://embeddedcomputing.me/en/meco-2017

At the conference, I presented my paper titled High-level Test Data Generation for software-based Self-test in Microprocessors. The co-authors of the paper are: Atjom Jasnetski, Anton Tsertov and Raimund Ubar. The paper presents a new high-level fault model and test generation method for software-based self-test in Microprocessor. The model presented is derived directly from the instruction set of the given microprocessor. We proposed a high-level deterministic method and algorithm for test data generation for the control path of the Microprocessor, while for the data path, a pseudo-exhaustive test generation was proposed.

The two conferences were very useful to me as I received valuable feedbacks and also had opportunity to network. I am optimistic that this experience will help a great deal in my research.

Thank you

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