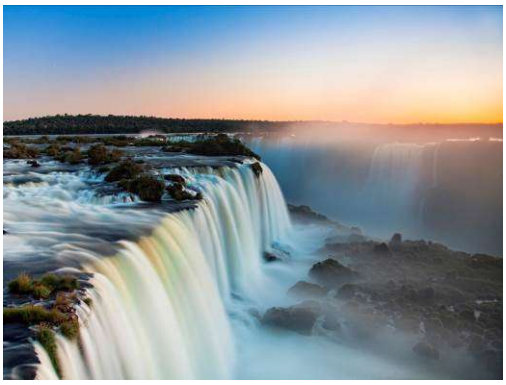
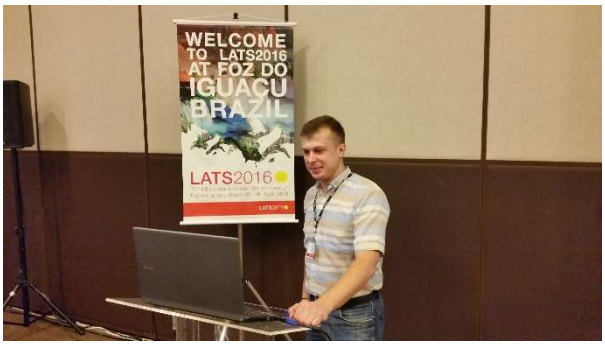
Sergei Kostin

17th IEEE Latin-American Test Symposium

The IEEE Latin-American Test Symposium (LATS, previously Latin-American Test Workshop - LATW) is a recognized forum for test and fault tolerance professionals and technologists from all over the world, in particular from Latin America, to present and discuss various aspects of system, board, and component testing and fault-tolerance with design, manufacturing and field considerations in mind.



LATS 2016 was taken place in the city of Foz do Iguaçu, Brazil, situated next to the famous falls on the Iguaçu River, which have a flow capacity equal to three times that of Niagara Falls. This year LATS offers an excellent technical program which covers contributions on fault simulation and modeling, automatic test generation, analog and mixed signal test, memory testing and fault injection, systemon-chip test, software-based fault tolerance, built-in self-test, issues on EMC, EMI and radiation, design verification and validation, as well as fault tolerant architectures. The program was supplemented with brilliant keynote and invited talks in highly important novel topics: “The Hype, Myths, and Realities of Testing 2.5D/3D Integrated Circuits”, “Accessing On-Chip Instruments through the System’s Life-Time, “Known Unknowns - Knowledge in the Presence of Unknowns“, “Transforming Nanodevices into Nanosystems: The N3XT 1,000X”, “Spin Transfer Torque Memories for On-chip Caches: Prospects and Perspectives”. Further, two interesting TTEP tutorials “Hierarchical Test for Today’s SOC and IoT“ and “Combining Structural and Functional Test Approaches Across System Levels“ were offered.



At the symposium I have presented a paper titled “Gate-Level Modelling of NBTI-Induced Delays Under Process Variations”, which was the result of a collaboration with our colleagues from Porto Alegre, Brazil. I had some feedback and discussions about next steps in our research topic on aging in nanoelectronics. Aging reduces the lifecycle of nanoelectonics devices and brings them to the wear-out phase much earlier due to physic effects appeared at ultimate scaling of transistors dimensions.

The conference gave a great opportunity to communicate with experts in different fields of microelectronics from industry, to get deeper overview of existing problems and possible solutions in industry as well as new trends in further ICs technology scaling.