LATS 2016

Artjom Jasnetski

PhD Student, TUT

The IEEE Latin-American Test Symposium (LATS) took place in the city of Foz do Iguaçu situated next to the famous falls on the Iguaçu River. It's a recognized forum for test and fault tolerance professionals and technologists from all over the world, to present and discuss various aspects of system, board, and component testing and fault-tolerance with design, manufacturing and field considerations in mind.

Symposium was 4 days long, composed from 10 Regular Paper Sessions, 2 Special Sessions, 1 Poster Session, 1 Keynote Address, 2 Panels, 4 Invited Talks and 2 TTEP Tutorials. The topics of sessions were on fault simulation and modeling, automatic test generation, analog and mixed signal test, memory testing and fault injection, system on-chip test, software-based fault tolerance, built-in self-test, issues on EMC, EMI and radiation, design verification and validation, as well as fault tolerant architectures.

Interesting keynotes were: "The Hype, Myths, and Realities of Testing 2.5D/3D Integrated Circuits" by Krishnendu, "Accessing On-Chip Instruments through the System's Life-Time", by Erik Larsson, "Known Unknowns - Knowledge in the Presence of Unknowns", by Bernd Becker, "Transforming Nanodevices into Nanosystems: The N3XT 1,000X" by Subhasish Mitra.

The final day was dedicated to TTEP tutorial, which consisted from very relevant presentations to my topic. "Combining Structural and Functional Test Approaches Across System Levels" presentation was a combination of different points of view to the testing, from microprocessor level test to board level test.