10th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC 2015)

This year it was the 10th edition of the ReCoSoc 2015 Symposium which was held in Bremen, Germany. There were a total of five sessions distributed through the 3 days of the event. The main focus of the publications accepted in this event were related to Reconfigurable architectures for System-on-Chips. Our paper titled "Automated minimisation of concurrent online checkers for Networks-on-Chip" was presented in the second day in the section of Network-on-Chip. In this paper we had tried to automize the process of introduction of hardware checkers for digital circuits (in our case a Network-on-Chip router) with the aim of achieving high fault coverage, while keeping the area consumption at an acceptable range at the same time. On the last day during a panel discussion, a view and plan of the next 10 years of ReCoSoC Symposium was discussed. And finally, there was also a Xilinx talk, which also was accompanied by a Xilinx workshop for acquiring further information regarding working with FPGA devices and tools. In total, it was a great opportunity for us, including me as a first year PhD student to attend different conferences and have a publication in them, which would open new windows to have further discussion with other researchers, PhD students and professors in the same field of research.

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